D:Wave
The Quantum Computing Company™

QPU-Specific Physical Properties: Advantage_system4.1

USER MANUAL

2021-09-27

Overview

This document describes the physical properties of a particular D-Wave QPU. It includes a summary of its physical properties and graphed data showing the anneal schedule and other details.

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D-Wave User Manual 09-1262A-A

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1 About this Document

1.1 Intended Audience

This document is for users of the D-Wave quantum computer system who want to better understand and leverage the physical implementation of the quantum processing unit (QPU) architecture. It assumes that readers have a background in quantum annealing and are familiar with Ising problem formulations.

1.2 Scope

This document describes the physical properties of a particular calibrated QPU. It includes a summary of its physical properties and graphed data showing the anneal schedule and other details.

Note: The values provided in this document are the physical properties of a calibrated QPU. They are not product specifications.

1.3 Related Documentation

Use this document in conjunction with the following other documents:

- *Getting Started with D-Wave Solvers*—Introduces the D-Wave system.
- *QPU Solver Datasheet*—Defines terms, provides in-depth background information on the D-Wave QPU, the quantum annealing process, ICE effects, and timing.
- *Solver Properties and Parameters Reference*—Describes the solver properties and parameters that are passed to and from QPUs and other solvers via the Solver API.

2 QPU Properties

2.1 System Identification

All data presented in this document are specific to the **Advantage_system4.1** solver.

2.2 Summary of Physical Properties

This table lists the physical properties of the calibrated QPU.

Table 2.1: QPU Physical Properties

Parameter	Value
Model	Advantage, performance update
Graph size	P16
Qubits	5627
Couplers	40279
Qubit temperature (mK)	15.4 ± 0.1
M_{AFM} (pH)[1]	1.647
Quantum critical point (GHz)	1.391
L_q (pH)[2]	371.683
C_q (fF)[3]	118.606
I_c (μA)[4]	2.099
Average single qubit thermal width (Ising units)	0.198
FM problem freezeout (scaled time)	0.064
Single qubit freezeout (scaled time)	0.612
Φ^i_{CCJJ} (Φ_0)[5]	-0.621
Φ^f_{CCJJ} (Φ_0)[6]	-0.717
Annealing time range (μs)	0.5 to 2000.0
Readout time range (μs)[7]	18.0 to 235.0
Programming time (μs)[8]	~ 7700
QPU delay time per sample (μs)	21.0
Readout error rate[9]	≤ 0.001

[1] Maximum available mutual inductance achievable between pairs of flux qubit bodies.
[2] Qubit inductance.
[3] Qubit capacitance.
[4] Qubit critical current.
[5] Initial value of the external flux applied to qubit compound Josephson-junction structures at the start of an anneal (s=0).
[6] Final value at the end of an anneal (s=1).
[7] Typical readout times for reading between one qubit and the full QPU.
[8] Typical for problems run on this QPU. Actual problem programming times may vary slightly depending on the nature of the problem.
[9] Error rate when reading the full system.

Note: In addition to the above list of physical properties, each QPU has a number of other properties defined in software that are accessible via the Solver API. For a global list of the solver properties for a QPU, and for a list of the permitted user parameters for each type of solver, see Solver Properties and Parameters. To retrieve the solver properties for a particular QPU, see the Ocean documentation for the syntax and examples.

2.3 Working Graph

The Advantage™ QPU is based on a physical lattice of qubits and couplers known as *Pegasus*. The Pegasus architecture comprises a repeated structure wherein each qubit is coupled to twelve oppositely aligned, and three similarly aligned, qubits. A basic unit cell contains twenty-four such qubits, with each qubit coupled to one similarly aligned qubit in the cell and two similarly aligned qubits in adjacent cells. As a whole, the Advantage QPU is a lattice of 16x16 such tiles, denoted as a *P16* graph. The global structure can be seen as a system of diagonally arranged K4,4 bicliques, with couplers between oppositely aligned qubits both within and between the diagonals. For more information on the Pegasus topology, see Getting Started with D-Wave Solvers.

Each Advantage QPU is fabricated with more than 5000 qubits and more than 35,000 couplers. Of this total, the number of devices, and the specific set of devices, that can be made available in the graph might change during a system cooldown and calibration cycle. The subset of the graph available to users is the *working graph.* The *yield* of the working graph is the percentage of working qubits that are present.

You can retrieve the sets of active qubits (`nodelist`) and couplers (`edgelist`) for this QPU using the Ocean tools. For more information, see Ocean documentation.

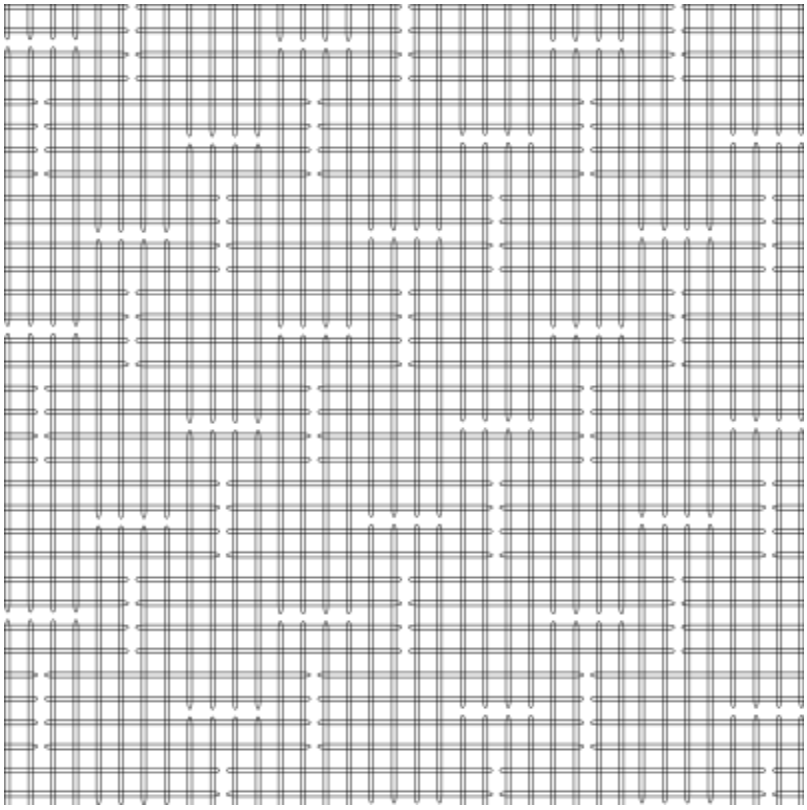

Figure 2.1: A cropped view of the ideal Pegasus topology with qubits represented as horizontal and vertical loops. Shown here are approximately three rows of 12 vertical qubits and three columns of 12 horizontal qubits for a total of 72 qubits, 36 vertical and 36 horizontal. This figure shows a portion of the ideal topology and does not represent a particular QPU.

2.4 Annealing Schedule

The following equation shows the quantum Hamiltonian that governs the annealing process, where $\hat{\sigma}_{x,z}^{(i)}$ are Pauli matrices operating on a qubit q_i and nonzero values of h_i and $J_{i,j}$ are limited to those available in the graph.

$$\mathcal{H}_{\text{ising}} = -\frac{A(s)}{2}\left(\sum_i \hat{\sigma}_x^{(i)}\right) + \frac{B(s)}{2}\left(\sum_i h_i \hat{\sigma}_z^{(i)} + \sum_{i>j} J_{i,j}\hat{\sigma}_z^{(i)}\hat{\sigma}_z^{(j)}\right) \tag{2.1}$$

The annealing schedule for this QPU is shown in Figure 2.2.

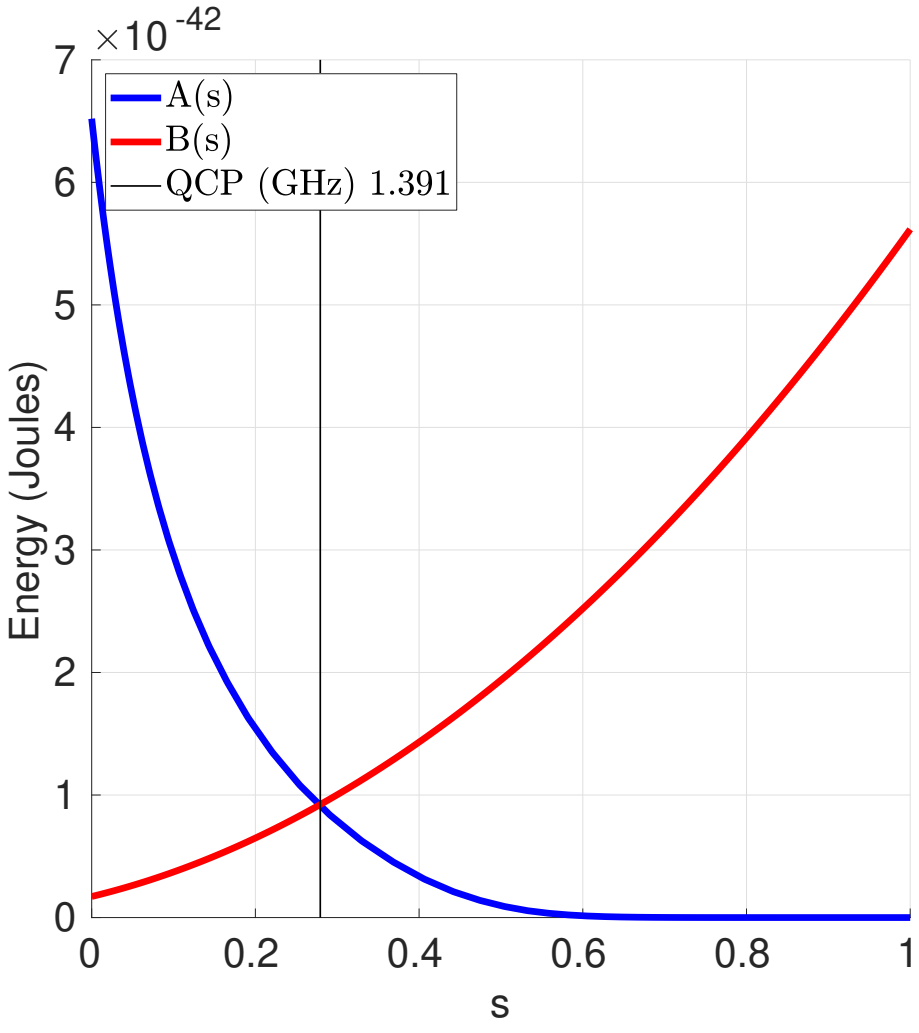

Figure 2.2: Annealing schedule for the QPU, showing energy changes as a function of scaled time.

2.5 DAC Quantization Effects

The on-QPU digital-analog converters (DACs) that provide the user-specified h and J values have a finite quantization step size. That step size depends on the value of the h and J applied because the response to the DAC output is nonlinear.

Figure 2.3 and Figure 2.4 show the effects of the DAC quantization step for the DACs controlling the h and J values, respectively, for this system.

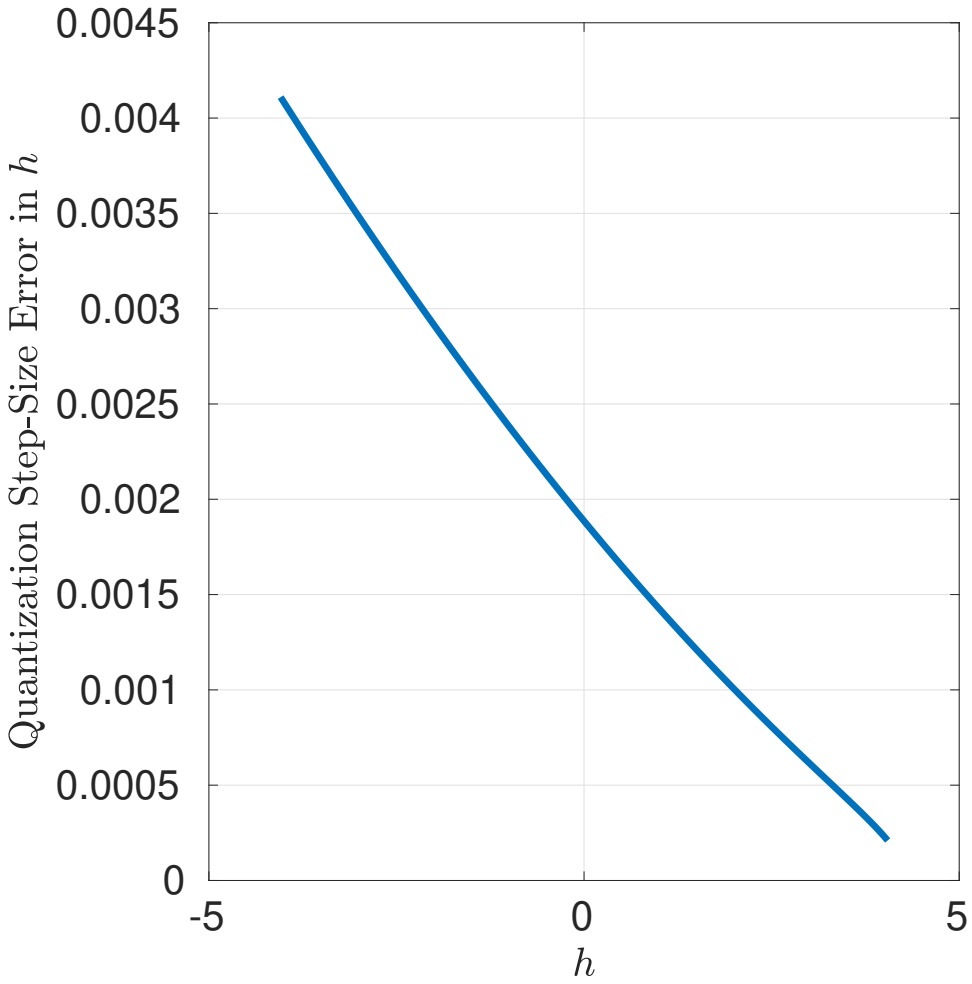

Figure 2.3: Typical quantization on the h DAC control.

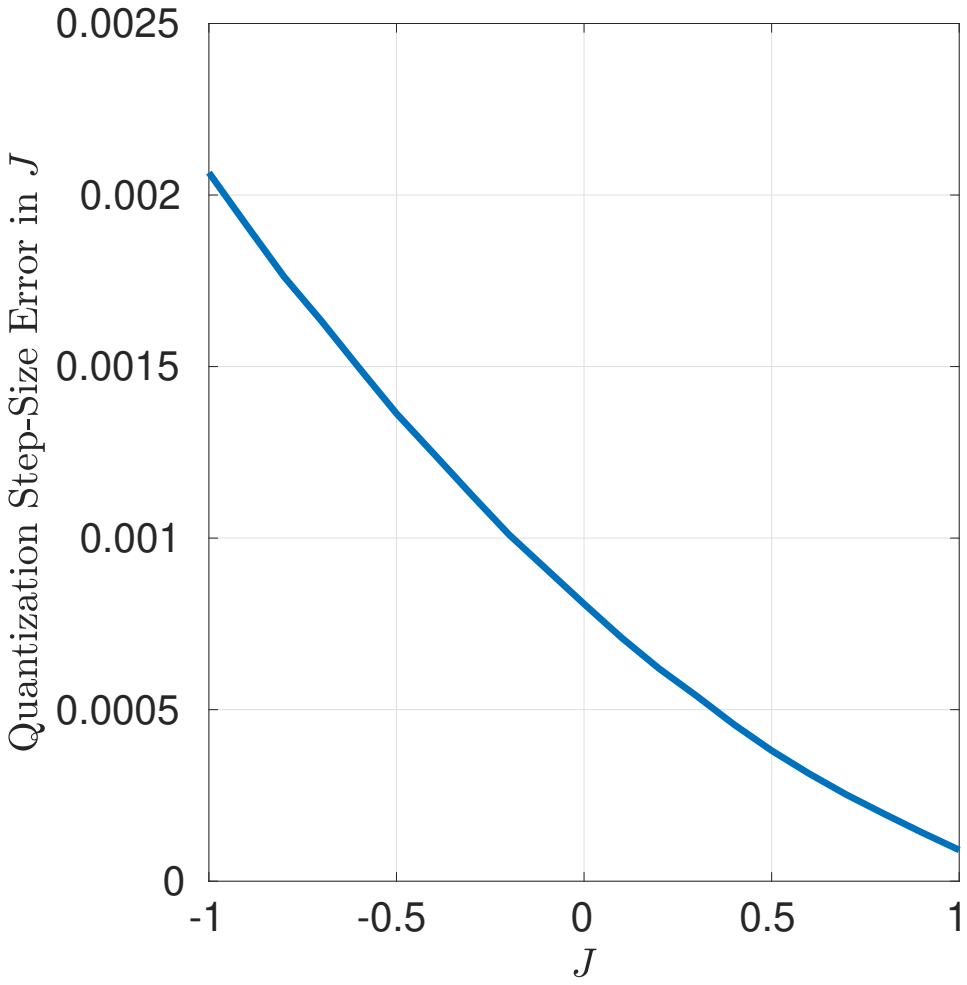

Figure 2.4: Typical quantization on the J DAC control.