



QPU-Specific Physical Properties: Advantage_system5.2

USER MANUAL

2022-07-11

Overview

This document describes the physical properties of a particular D-Wave QPU. It includes a summary of its physical properties and graphed data showing the anneal schedule and other details.

CONTACT

Corporate Headquarters
3033 Beta Ave
Burnaby, BC V5G 4M9
Canada
Tel. 604-630-1428

US Office
2650 E Bayshore Rd
Palo Alto, CA 94303

Email: info@dwavesys.com

www.dwavesys.com

Notice and Disclaimer

D-Wave Systems Inc. (D-Wave), its subsidiaries and affiliates, makes commercially reasonable efforts to ensure that the information in this document is accurate and up to date, but errors may occur. NONE OF D-WAVE SYSTEMS INC., its subsidiaries and affiliates, OR ANY OF ITS RESPECTIVE DIRECTORS, EMPLOYEES, AGENTS, OR OTHER REPRESENTATIVES WILL BE LIABLE FOR DAMAGES, CLAIMS, EXPENSES OR OTHER COSTS (INCLUDING WITHOUT LIMITATION LEGAL FEES) ARISING OUT OF OR IN CONNECTION WITH THE USE OF THIS DOCUMENT OR ANY INFORMATION CONTAINED OR REFERRED TO IN IT. THIS IS A COMPREHENSIVE LIMITATION OF LIABILITY THAT APPLIES TO ALL DAMAGES OF ANY KIND, INCLUDING (WITHOUT LIMITATION) COMPENSATORY, DIRECT, INDIRECT, EXEMPLARY, PUNITIVE AND CONSEQUENTIAL DAMAGES, LOSS OF PROGRAMS OR DATA, INCOME OR PROFIT, LOSS OR DAMAGE TO PROPERTY, AND CLAIMS OF THIRD PARTIES.

D-Wave reserves the right to alter this document and other referenced documents without notice from time to time and at its sole discretion. D-Wave reserves its intellectual property rights in and to this document and its proprietary technology, including copyright, trademark rights, industrial design rights, and patent rights. D-Wave trademarks used herein include D-Wave™, Leap™, Ocean™, Advantage™, Advantage2™, D-Wave 2000Q™, D-Wave 2X™, D-Wave Learn™, D-Wave Launch™, and the D-Wave logos (the D-Wave Marks). Other marks used in this document are the property of their respective owners. D-Wave does not grant any license, assignment, or other grant of interest in or to the copyright of this document, the D-Wave Marks, any other marks used in this document, or any other intellectual property rights used or referred to herein, except as D-Wave may expressly provide in a written agreement. This document may refer to other documents, including documents subject to the rights of third parties. Nothing in this document constitutes a grant by D-Wave of any license, assignment, or any other interest in the copyright or other intellectual property rights of such other documents. Any use of such other documents is subject to the rights of D-Wave and/or any applicable third parties in those documents.

Contents

1	About this Document	1
1.1	Intended Audience	1
1.2	Scope	1
1.3	Related Documentation	1
2	QPU Properties	2
2.1	System Identification	2
2.2	Summary of Physical Properties	2
2.3	Working Graph	3
2.4	Annealing Schedule	5
2.5	DAC Quantization Effects	6

1 About this Document

1.1 Intended Audience

This document is for users of the D-Wave quantum computer system who want to better understand and leverage the physical implementation of the quantum processing unit (QPU) architecture. It assumes that readers have a background in quantum annealing and are familiar with Ising problem formulations.

1.2 Scope

This document describes the physical properties of a particular calibrated QPU. It includes a summary of its physical properties and graphed data showing the anneal schedule and other details.

Note: The values provided in this document are the physical properties of a calibrated QPU. They are not product specifications.

1.3 Related Documentation

Use this document in conjunction with the following other documents:

- [Getting Started with D-Wave Solvers](#)—Introduces the D-Wave system.
- [QPU Solver Datasheet](#)—Defines terms, provides in-depth background information on the D-Wave QPU, the quantum annealing process, ICE effects, and timing.
- [Solver Properties and Parameters Reference](#)—Describes the solver properties and parameters that are passed to and from QPUs and other solvers via the Solver API.

2 QPU Properties

2.1 System Identification

All data presented in this document are specific to the **Advantage_system5.2** solver.

2.2 Summary of Physical Properties

This table lists the physical properties of the calibrated QPU.

Table 2.1: QPU Physical Properties

Parameter	Value
Model	Advantage, performance update
Graph size	P16
Qubits	5617
Couplers	40087
Qubit temperature (mK) ¹	16.4 ± 0.1
M_{AFM} (pH) ²	1.687
Quantum critical point (GHz)	1.389
L_q (pH) ³	374.770
C_q (fF) ⁴	117.013
I_c (μA) ⁵	2.101
Average single qubit thermal width (Ising units)	0.193
FM problem freezeout (scaled time)	0.067
Single qubit freezeout (scaled time)	0.622
Φ_{CCJ}^i (Φ_0) ⁶	-0.620
Φ_{CCJ}^f (Φ_0) ⁷	-0.714
Annealing time range (μs)	0.5 to 2000.0
Readout time range (μs) ⁸	18.0 to 123.0
Programming time (μs) ⁹	~ 13300
QPU delay time per sample (μs)	21.0
Readout error rate ¹⁰	≤ 0.001

¹ Some qubits in this QPU are affected by high-frequency photon flux and may have a higher temperature than what is reported here. For more information, see the discussion of high-energy photon flux in [QPU Solver Datasheet](#).

² Maximum available mutual inductance achievable between pairs of flux qubit bodies.

³ Qubit inductance.

⁴ Qubit capacitance.

⁵ Qubit critical current.

⁶ Initial value of the external flux applied to qubit compound Josephson-junction structures at the start of an anneal (s=0).

⁷ Final value at the end of an anneal (s=1).

⁸ Typical readout times for reading between one qubit and the full QPU.

⁹ Typical for problems run on this QPU. Actual problem programming times may vary slightly depending on the nature of the problem.

¹⁰ Error rate when reading the full system.

Note: In addition to the above list of physical properties, each QPU has a number of other properties defined in software that are accessible via the Solver API. For a global list of the solver properties for a QPU, and for a list of the permitted user parameters for each type of solver, see [Solver Properties and Parameters](#). To retrieve the solver properties for a particular QPU, see the [Ocean documentation](#) for the syntax and examples.

2.3 Working Graph

The Advantage™ QPU is based on a physical lattice of qubits and couplers known as *Pegasus*. The Pegasus architecture comprises a repeated structure wherein each qubit is coupled to twelve oppositely aligned, and three similarly aligned, qubits. A basic unit cell contains twenty-four such qubits, with each qubit coupled to one similarly aligned qubit in the cell and two similarly aligned qubits in adjacent cells. As a whole, the Advantage QPU is a lattice of 16x16 such tiles, denoted as a *P16* graph. The global structure can be seen as a system of diagonally arranged K4,4 bicliques, with couplers between oppositely aligned qubits both within and between the diagonals. For more information on the Pegasus topology, see [Getting Started with D-Wave Solvers](#).

Each Advantage QPU is fabricated with more than 5000 qubits and more than 35,000 couplers. Of this total, the number of devices, and the specific set of devices, that can be made available in the graph might change during a system cooldown and calibration cycle. The subset of the graph available to users is the *working graph*. The *yield* of the working graph is the percentage of working qubits that are present.

You can retrieve the sets of active qubits (`odelist`) and couplers (`edgelist`) for this QPU using the Ocean tools. For more information, see [Ocean documentation](#).

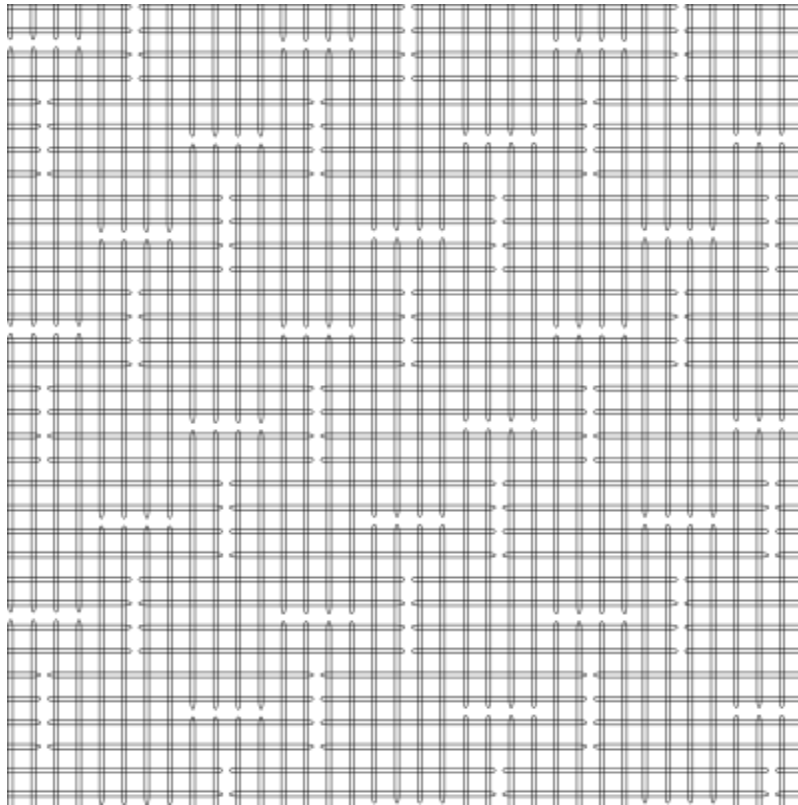


Figure 2.1: A cropped view of the ideal Pegasus topology with qubits represented as horizontal and vertical loops. Shown here are approximately three rows of 12 vertical qubits and three columns of 12 horizontal qubits for a total of 72 qubits, 36 vertical and 36 horizontal. This figure shows a portion of the ideal topology and does not represent a particular QPU.

2.4 Annealing Schedule

The following equation shows the quantum Hamiltonian that governs the annealing process, where $\hat{\sigma}_{x,z}^{(i)}$ are Pauli matrices operating on a qubit q_i and nonzero values of h_i and $J_{i,j}$ are limited to those available in the graph.

$$\mathcal{H}_{\text{ising}} = -\frac{A(s)}{2} \left(\sum_i \hat{\sigma}_x^{(i)} \right) + \frac{B(s)}{2} \left(\sum_i h_i \hat{\sigma}_z^{(i)} + \sum_{i>j} J_{i,j} \hat{\sigma}_z^{(i)} \hat{\sigma}_z^{(j)} \right) \tag{2.1}$$

The annealing schedule for this QPU is shown in Figure 2.2.

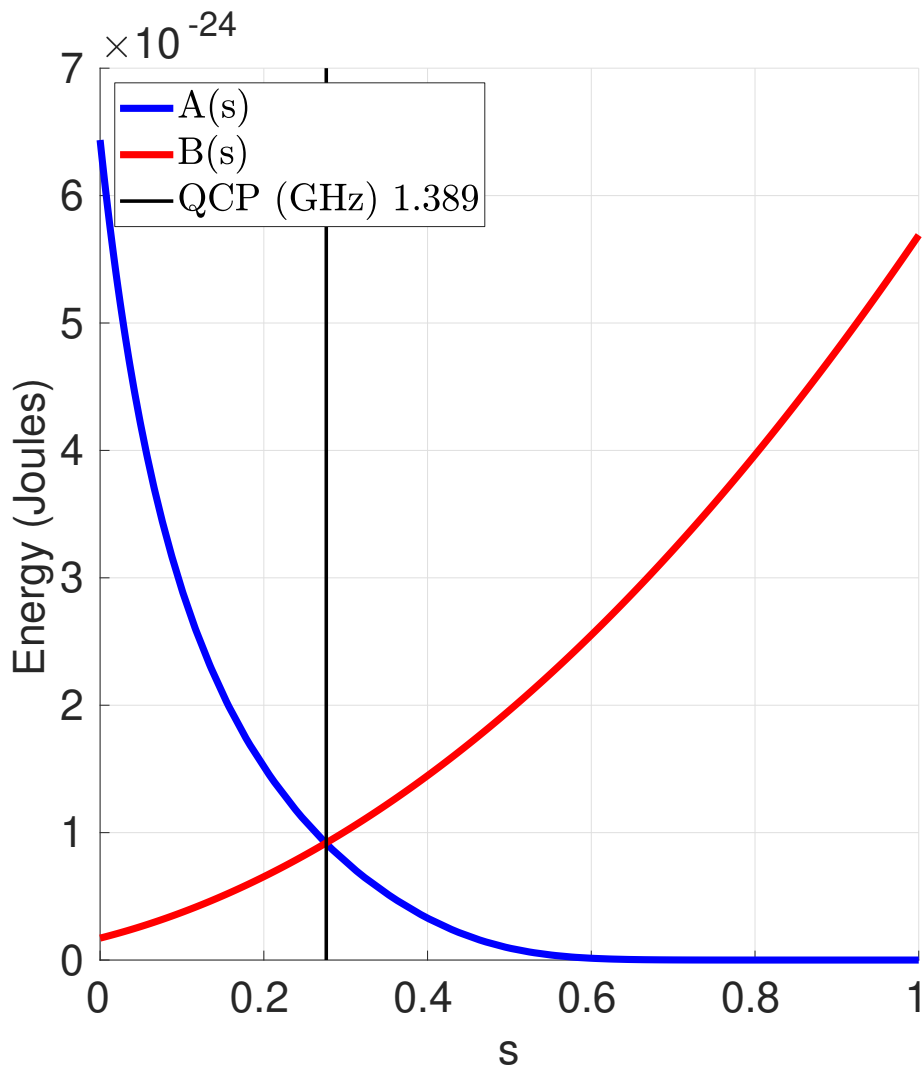


Figure 2.2: Annealing schedule for the QPU, showing energy changes as a function of scaled time.

2.5 DAC Quantization Effects

The on-QPU digital-analog converters (DACs) that provide the user-specified h and J values have a finite quantization step size. That step size depends on the value of the h and J applied because the response to the DAC output is nonlinear.

Figure 2.3 and Figure 2.4 show the effects of the DAC quantization step for the DACs controlling the h and J values, respectively, for this system.

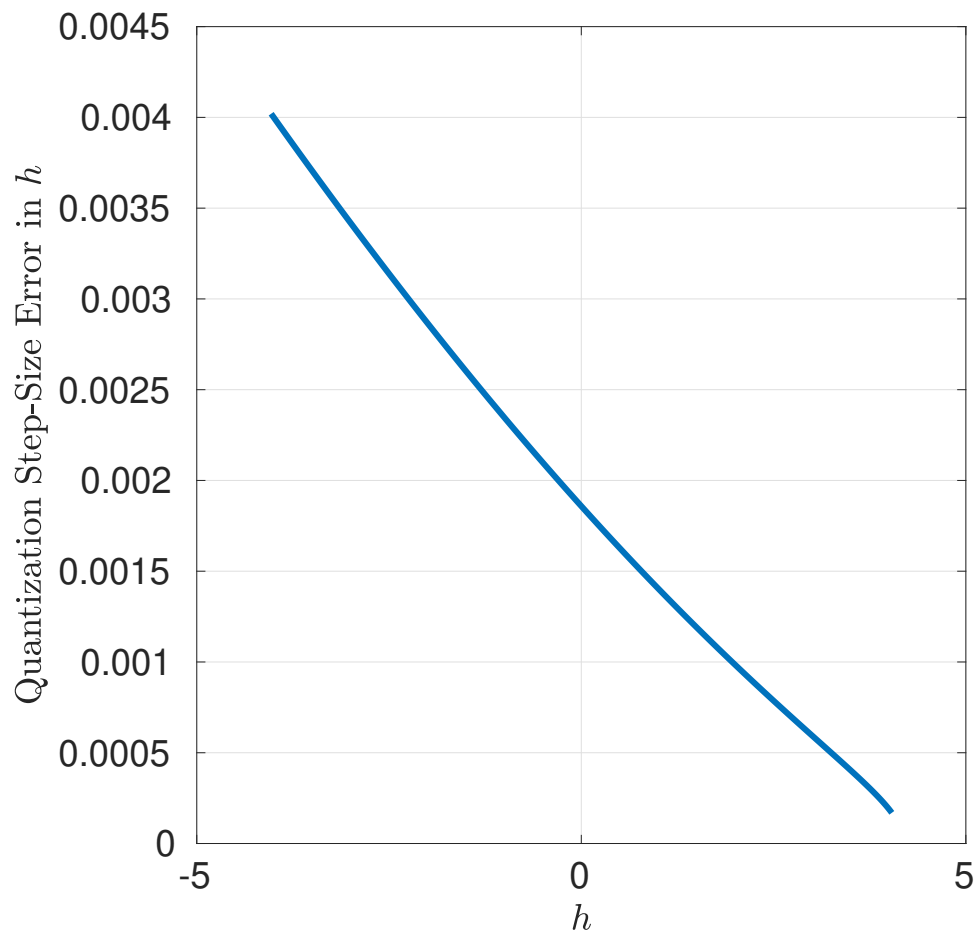


Figure 2.3: Typical quantization on the h DAC control.

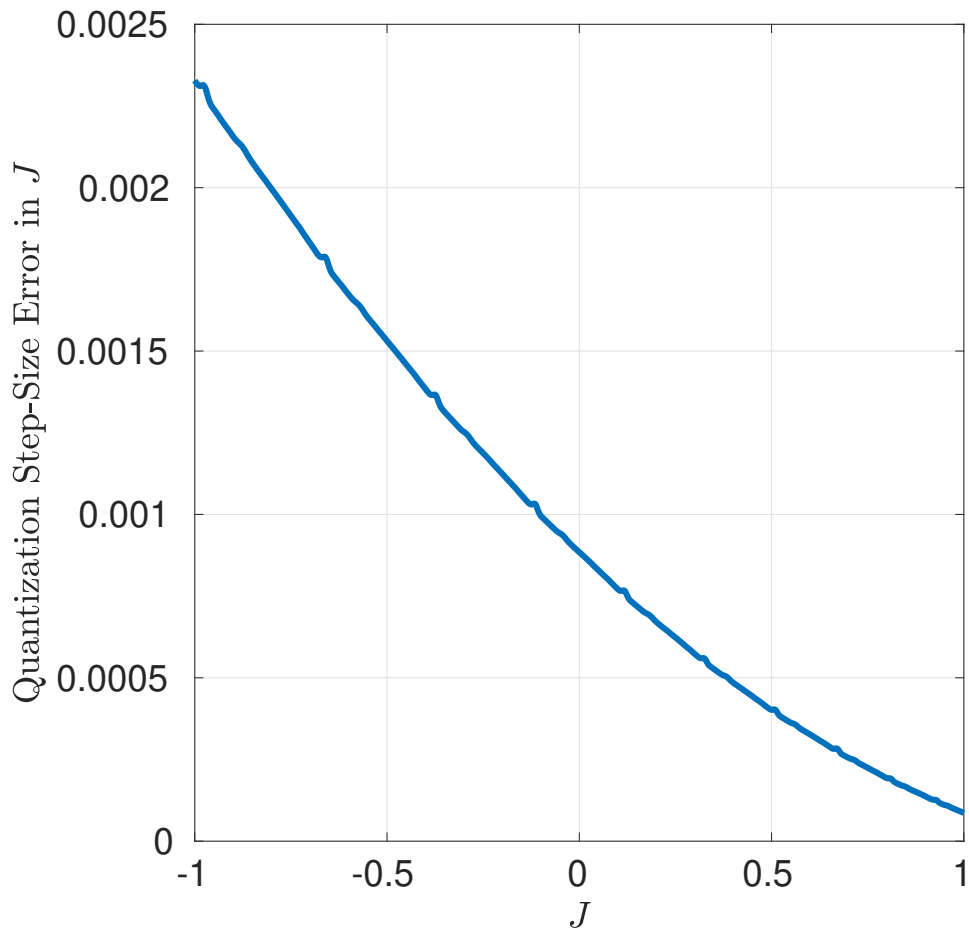


Figure 2.4: Typical quantization on the J DAC control.